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- 1** Techniques for obtaining high performance in Java programs 88%

Iffat H. Kazi , Howard H. Chen , Berdenia Stanley , David J. Lilja  
**ACM Computing Surveys (CSUR)** September 2000  
 Volume 32 Issue 3  
 This survey describes research directions in techniques to improve the performance of programs written in the Java programming language. The standard technique for Java execution is interpretation, which provides for extensive portability of programs. A Java interpreter dynamically executes Java bytecodes, which comprise the instruction set of the Java Virtual Machine (JVM). Execution time performance of Java programs can be improved through compilation, possibly at the expense of portabili ...
- 2** A brief history of just-in-time 87%

John Aycock  
**ACM Computing Surveys (CSUR)** June 2003  
 Volume 35 Issue 2  
 Software systems have been using "just-in-time" compilation (JIT) techniques since the 1960s. Broadly, JIT compilation includes any translation performed dynamically, after a program has started execution. We examine the motivation behind JIT compilation and constraints imposed on JIT compilation systems, and present a classification scheme for such systems. This classification emerges as we survey forty years of JIT work, from 1960--2000.
- 3** Efficient Java exception handling in just-in-time compilation 85%

Seungll Lee , Byung-Sun Yang , Suhyun Kim , Seongbae Park , Soo-Mook Moon , Kemal Ebcioglu , Erik Altman  
**Proceedings of the ACM 2000 conference on Java Grande** June 2000

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L24 and java

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side by side

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<u>L25</u>	L24 and java	1	<u>L25</u>
<u>L24</u>	(revert\$ near5 instruction\$)	140	<u>L24</u>
<u>L23</u>	l4 and (rever\$ or oppos\$)	0	<u>L23</u>
<u>L22</u>	l4 and (memory\$ or data or cache\$)	1	<u>L22</u>
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<u>L20</u>	l4 and (load\$ OR STOR\$)	1	<u>L20</u>
<u>L19</u>	l4 and load\$ OR STOR\$	1083749	<u>L19</u>
<u>L18</u>	l4 and (except\$ or error\$ or signal\$)	0	<u>L18</u>
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<u>L14</u>	l4 and (operand or depth\$ or stack\$)	1	<u>L14</u>
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<u>L12</u>	(sipush or bipush) same (overflow\$ or underflow\$)	0	<u>L12</u>
<u>L11</u>	(sipush or bipush) near5 (overflow\$ or underflow\$)	0	<u>L11</u>
<u>L10</u>	l1 and sipush and bipush	0	<u>L10</u>

<u>L9</u>	l4 and (overflow\$ or underflow\$)	0	<u>L9</u>
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<i>DB=USPT,USOC; PLUR=YES; OP=ADJ</i>			
<u>L6</u>	l4 and overflow\$ and underflow\$	0	<u>L6</u>
<u>L5</u>	l1 and overflow\$ and underflow\$	1	<u>L5</u>
<i>DB=USPT; PLUR=YES; OP=ADJ</i>			
<u>L4</u>	5875336.pn.	1	<u>L4</u>
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<u>L2</u>	L1 and (execut\$ near5 stack\$)	1	<u>L2</u>
<u>L1</u>	6332215.pn.	1	<u>L1</u>

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### 1 Techniques for obtaining high performance in Java programs 99%



Iffat H. Kazi , Howard H. Chen , Berdenia Stanley , David J. Lilja

**ACM Computing Surveys (CSUR)** September 2000

Volume 32 Issue 3

This survey describes research directions in techniques to improve the performance of programs written in the Java programming language. The standard technique for Java execution is interpretation, which provides for extensive portability of programs. A Java interpreter dynamically executes Java bytecodes, which comprise the instruction set of the Java Virtual Machine (JVM). Execution time performance of Java programs can be improved through compilation, possibly at the expense of portability ...

### 2 Improving Java performance using hardware translation 94%



Ramesh Radhakrishnan , Ravi Bhargava , Lizy K. John

**Proceedings of the 15th international conference on Supercomputing** June 2001

State of the art Java Virtual Machines with Just-In-Time (JIT) compilers make use of advanced compiler techniques, run-time profiling and adaptive compilation to improve performance. However, these techniques for alleviating performance bottlenecks are more effective in long running workloads, such as server applications. Short running Java programs, or client workloads, spend a large fraction of their execution time in compilation instead of useful execution when run using JIT compilers. In ...

### 3 LLVA: A Low-level Virtual Instruction Set Architecture 92%



Vikram Adve , Chris Lattner , Michael Brukman , Anand Shukla , Brian Gaeke

**Proceedings of the 36th Annual IEEE/ACM International Symposium on**

**Microarchitecture** December 2003

A virtual instruction set architecture (V-ISA) implemented via a processor-specific

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☐ Check to search within this result set**Results Key:****JNL** = Journal or Magazine   **CNF** = Conference   **STD** = Standard**1 Early load address resolution via register tracking**

*Bekeman, M.; Yoaz, A.; Gabbay, F.; Jourdan, S.; Kalaev, M.; Ronen, R.;*  
 Computer Architecture, 2000. Proceedings of the 27th International Symposium on , 10-14 June 2000  
 Pages:306 - 315

[\[Abstract\]](#)   [\[PDF Full-Text \(964 KB\)\]](#)   **IEEE CNF**
**2 An X86 microprocessor with multimedia extensions**

*Draper, D.A.; Crowley, M.P.; Holst, J.; Favor, G.; Schoy, A.; Ben-Meir, A.; Tru Khanna, R.; Wendell, D.; Krishna, R.; Nolan, J.; Partovi, H.; Johnson, M.; Lee Mallick, D.; Frydel, G.; Vuong, A.; Yu, S.; Maley, R.; Kauffmann, B.;*  
 Solid-State Circuits Conference, 1997. Digest of Technical Papers. 44th ISSCC 1997 IEEE International , 6-8 Feb. 1997  
 Pages:172 - 173, 450

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<u>L12</u>	717/146,147,148,149.ccls.	411	<u>L12</u>
<u>L11</u>	717/136,137,138,139,140.ccls.	494	<u>L11</u>
<i>DB=TDBD; PLUR=YES; OP=ADJ</i>			
<u>L10</u>	L8	0	<u>L10</u>
<i>DB=DWPI; PLUR=YES; OP=ADJ</i>			
<u>L9</u>	L8	0	<u>L9</u>
<i>DB=JPAB; PLUR=YES; OP=ADJ</i>			
<u>L8</u>	cpu and (register\$ near4 instruction\$) and (stack\$ near5 instruction\$) and (translat\$ or decod\$ or compil\$)and overflow\$ and underflow\$	0	<u>L8</u>
<i>DB=EPAB; PLUR=YES; OP=ADJ</i>			
<u>L7</u>	cpu and (register\$ near4 instruction\$) and (stack\$ near5 instruction\$) and (translat\$ or decod\$ or compil\$)and overflow\$ and underflow\$	0	<u>L7</u>



*DB=USOC; PLUR=YES; OP=ADJ*

L6    cpu and (register\$ near4 instruction\$) and (stack\$ near5 instruction\$) and  
       (translat\$ or decod\$ or compil\$)and overflow\$ and underflow\$

2 L6

*DB=PGPB; PLUR=YES; OP=ADJ*

L5    cpu and (register\$ near4 instruction\$) and (stack\$ near5 instruction\$) and  
       (translat\$ or decod\$ or compil\$)and overflow\$ and underflow\$

14 L5

*DB=USPT; PLUR=YES; OP=ADJ*

L4 L3 and java

17 L4

L3 L2 and exception\$

162 L3

**L2** L1 and overflow\$ and underflow\$

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L1    cpu and (register\$ near4 instruction\$) and (stack\$ near5 instruction\$) and  
       (translat\$ or decod\$ or compil\$)

941 L1

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